PRINTER RUSH

(PTO ASSISTANCE)

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[RUSH] **MESSAGE:** Specification: page 15 Line # 28 Application Serial No. 09/_____ is missing, please resolve.

*There is nothing missing on page 15 line 28.

Page 12 there is a serial number missing Pgs (PUBS) Thank you.

[XRUSH] **RESPONSE:**

DNE

INITIALS: tyl

NOTE: This form will be included as part of the official USPTO record, with the Response document coded as XRUSH.

REV 10/04

The charging time-constant of the resistor **502** and capacitor **503** combination is selected to prevent voltage **510** from reaching the trip level **511** of Comparator **506** during a "0" time period. When a "0" clock edge **540** of **FIG. 6** occur, SPI Data-Out **515** to the Peripheral Device **600** a "0" can be clocked in. In a like manner, the time period for a "1" is long enough to ensure that the Comparator **504** trip level **511** is reached before the clock edge **540 FIG. 7** occurs and a "1" is clocked in.

In order to hold the most recent "bit" value for use by Asynchronous type Peripheral Devices, the Comparator **504** output **517** is applied as input to NAND gate **507** and its inverted state, via Inverter **521,** is applied to the input of NAND gate **519**. While the Data-Out + Clock signal **301** is low, the pull-down resistor **508** holds the second input of NAND gates **519** and **507** low keeping their respective outputs **533** and **531** high. As the Data-Out + Clock signal **301** (or **401**) goes high at the end of a bit period, voltage **516** is also pulled high for a period, controlled by the time constant of resistor **508** and capacitor **506**, briefly enabling NAND gates **519** and **507,** thus enabling the flip-flop made up of NAND gates **523** and **524** to latch the state of **517** as follows: (A) if voltage **517** is high, the output of NAND gate **507** becomes low thus setting the flip-flop made up of NAND gates **523** and **524** such that output **525** latches high representing a "1" Data-Out **525** for UART; and (B) in a similar manner, if signal **517** is low, the output of NAND gate **519** becomes low causing the flip-flop output **525** latches low, representing a "0" for UART Data-Out **525.**

Isolation circuitry 400 for electrically isolating high voltage inputs and outputs from the low voltage logic levels signals of the host may optionally but advantageously be provided between Data Direction Multiplexer **300** and Data-Out extractor 500. An embodiment of isolation circuitry **400** is show in **FIG. 9** and described in greater detail hereinbelow and in co-pending United States Patent Application Serial No. 09/915,188 filed 25 July 2001 (Attorney Docket No. A-70826/RMA) entitled *System, Device, And Method For Comprehensive Input/Output Interface Between Process Or Machine Transducers And Controlling Device Or System*. In the illustrated embodiment, Data-Out+Clock 311 passes